CLAIMS

What is claimed is:

1. A method for receiving asynchronous transfer mode (ATM) cells in a host from a client over a bus, comprising the steps of:

determining whether an ATM cell in said client is ready to be transferred over said bus to a storage device within said host; and

preventing overflow of said storage device by calculating a first available cell space in said storage device as a function of a write value, a read value image and a size value of said storage device.

2. The method of claim 1 further comprising the step of transferring an ATM cell from said client to said storage device.

3. The method of claim 1 further comprising the step of updating said read value image.

4. The method of claim 3, wherein said read value image updating is executed upon said first available cell space falling below a programmable level.

5. The method of claim 1, wherein underflow of said storage device is prevented by calculating a second available cell space in said storage device as a function of a read value, a write value image and a size value of said storage device.

6. The method of claim 5 further comprising the step of updating said write value image.

7. The method of claim 6, wherein said write value image updating is executed upon reaching a programmable number of transferred ATM cells.

8. The method of claim 1, wherein said write value and read value image are specified by pointers associated with a storage device within said client.

9. The method of claim 5, wherein said read value and write value image are specified by pointers associated with said storage device.

10. A method for transmitting asynchronous transfer mode (ATM) cells from a host to a client over a bus, comprising the steps of:

determining whether an ATM cell in a storage device within said host is ready to be transferred over said bus to said client; and

preventing overflow of said storage device by calculating a first available cell space in said storage device as a function of a write value, a read value image and a size value of said storage device.

11. The method of claim 10 further comprising the step of transferring an ATM cell from said storage device to said client.

12. The method of claim 10 further comprising the step of updating said read value image.

13. The method of claim 12, wherein said read value image updating is executed upon reaching a programmable number of transferred ATM cells.

14. The method of claim 10, wherein underflow of said storage device is prevented by calculating a second available cell space in said storage device as a function of a read value, a write value image and a size value of said storage device.

15. The method of claim 14 further comprising the step of updating said write value image.

16. The method of claim 10, wherein said write value and read value image are specified by pointers associated with said storage device.

17. The method of claim 15, wherein said write value image updating is executed upon falling under a programmable level of said second available cell space.

18. The method of claim 14, wherein said read value and write value image are specified by pointers associated with a storage device within said client.

19. A system for receiving asynchronous transfer mode (ATM) cells over a bus, comprising:

a host comprising a receiver data sink for storing ATM cells to be received, and a computer program for preventing overflow of said receiver data sink by calculating a first available cell space of said receiver data sink as a function of a read value, a write value image and a size value of said receiver data sink; and

a client comprising a receiver data source for storing ATM cells to be transferred, and a finite state machine for calculating a second available cell space of said receiver data sink as a function of a write value, a read value image and a size value of said receiver data sink in order to prevent underflow of said receiver data source.

20. The apparatus of claim 19, wherein said read value image is updated upon said second available cell space falling below a programmable level.

21. The apparatus of claim 20, whereby said updating is controlled and initiated by said host.

22. The apparatus of claim 19, wherein said write value image is updated upon reaching a programmable number of transferred ATM cells.

23. The apparatus of claim 22, whereby said updating is controlled and initiated by said host.

24. The apparatus of claim 19, wherein said write value and read value image are specified by pointers associated with said receiver data source and said read value and write value image are specified by pointers associated with said receiver data sink.

25. The apparatus of claim 19, wherein said receiver data sink is a ring buffer and said receiver data source is a FIFO memory.

26. The apparatus of claim 19, wherein said bus is a PCI bus.

27. An apparatus for transmitting asynchronous transfer mode (ATM) cells over a bus, comprising:

a host comprising a transmitter data source for storing ATM cells to be transferred, and a computer program for preventing overflow of said transmitter data source by calculating a first available cell space of said transmitter data source as a function of a write value, a read value image and a size value of said transmitter data source; and

a client comprising a transmitter data sink for storing ATM cells to be received, and a finite state machine for calculating a second available cell space of said transmitter data source as a function of a read value, a write value image and a size value of said transmitter data source in order to prevent underflow of said transmitter data source.

28. The apparatus of claim 27, wherein said read value image is updated upon reaching a programmable number of transferred ATM cells.

29. The apparatus of claim 28, whereby said updating is controlled and initiated by said host.

30. The apparatus of claim 27, wherein said write value image is updated upon falling said second available cell space below a programmable level.

31. The apparatus of claim 30, whereby said updating is controlled and initiated by said host.

32. The apparatus of claim 27, wherein said write value and read value image are specified by pointers associated with said transmitter data source and said read value and write value image are specified by pointers associated with said transmitter data sink.

33. The apparatus of claim 27, wherein said transmitter data source is a ring buffer and said transmitter data sink is a FIFO memory.

34. The apparatus of claim 27, wherein said bus is a PCI bus.